ABSTRACT

In a non-volatile passive matrix memory device (10) comprising an electrically polarizable dielectric memory material (12) exhibiting hysteresis, first and second sets (14;15) of addressing electrodes constitute word lines (WL) and bit lines (BL) of the memory device. A memory cell (13) is defined in the memory material (12) at the overlap between a word line (WL) and a bit line (BL). The word lines (WL) are divided into segments (S) with each segments sharing and being defined by adjoining bit lines (BL). Means (25) are provided for connecting each bit line (BL) of a segment (S) with a sensing means (26), thus enabling simultaneous connections of all memory cells (13) of a word line segment (15) for readout via the bit lines (BL) of the segment (S). Each sensing means (26) senses the charge flow in a bit line (BL) in order to determine a stored logical value. In a readout method a word line (WL) of a segment (S) is activated by setting its potential to a switching voltage V_s of the memory cell (13) during at least a portion of a read cycle, while keeping the bit lines (BL) of the segment (S) at zero potential, during which read cycle a logical value stored in the individual memory cells (13) is sensed by the sensing means (26). – Use in a volumetric data storage apparatus.

Fig. 5